Docket No.: 21806-00156-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kiran Chatty et al.

Confirmation No.: 2698

Application No.: 10/605,699

Filed: October 21, 2003

Art Unit: 2818

For: METHOD AND STRUCTURE TO SUPPRESS EXTERNAL LATCHUP

Examiner: David Vu

SUPPLEMENTAL APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 5, 2006

Dear Sir:

As required under § 41.37(a), this brief is timely filed within two months of the Notice of Appeal filed in this case on May 1, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

App. C Related Proceedings

I. REAL PARTY IN INTEREST

Real party in interest: International Business Machines Corporation, Burlington, VT USA.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application: There are 31 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: 32-51

3. Claims pending: 1-31

4. Claims allowed: None

5. Claims rejected: 1-31

C. Claims On Appeal: The claims on appeal are claims 1-31.

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Overview of Applicants' Claimed Invention

The present invention relates to a method and structure for protection against latch-up. Integrated circuits manufactured in accordance with the present disclosure feature well and substrate contacts of varying periodicity. Such a strategy enables maximizing the design of an integrated circuit as to the suppression of latch-up while concurrently optimizing available area

on the chip allocable to circuit design. The method and structure of the present invention is particularly beneficial to protect against cable discharge events and other discharge occurrences prone to injecting large current densities into an integrated circuit.

B. Detailed Summary of Claimed Invention with Reference to the Disclosure

A detailed discussion below is cross-referenced to the Specification and Figures is provided below as published in U.S. Patent Application Publication US 2005/0085028A1 (i.e., this application).

The present invention is a CMOS semiconductor structure comprising: a substrate; and a plurality of circuit structures formed upon the substrate. At least one of the circuit structures of the present invention has a susceptibility to a latch-up condition; an injection site associated with said CMOS semiconductor structure; and a plurality of contact regions that are inter-spaced at varying distances between said circuit structures. More specifically, FIG. 6A illustrates a plan view of the structure of the present invention as a portion of an integrated circuit (IC) **600** formed on substrate **590**. IC **600** includes groups (or regions) of contacts **601** of varying periodicity.[1]

In addition, FIG. 6A illustrates a portion of an integrated circuit **600** with contacts **601** arranged vertically. In the region of the IC near the injection site (i.e., I/O cell **602** and ESD diode **603**), the periodicity of contacts **601** is smaller than the periodicity utilized as distance is traversed away from the injection site. In particular, IC areas **604** include structures that may be susceptible to latch-up (e.g., internal circuits that include n-wells and p-wells).[2]

In order to avoid causing latch-up within circuit structures **604**, the quantity of contacts needed for circuit structures **604** near the injection site is made greater than for circuit structures **604** remote from the injection site. Specifically, the periodicity **L4** is greater than periodicity **L3**, which is greater than periodicity **L2**, which is greater than periodicity **L1**. The periodicity **L1** is smallest and a greater number of contacts occur for the periodicities **L2-L4**. Each of contacts

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[1] *Chatty et al.* at FIG. 6A; paragraph [0058], lines 1-5.
[2] *Id.* at FIG. 6A; paragraph [0058], lines 5-12.

601 represents multiple NWSX contact books the periodicities **L1-L4** define the distance between adjacent contacts **601**.[3]

Another embodiment of the present invention comprises a method for forming a semiconductor structure having improved latch-up robustness, the method comprising the steps of providing a substrate including an injection site and a plurality of circuit structures, wherein at least one of the circuit structures has a susceptibility to a latch-up condition; and forming a plurality of contact regions inter-spaced a varying distance between the circuit structures.

FIG. 5 illustrates a flow diagram of an embodiment of the invention presenting steps performed in designing and manufacturing an IC having contacts of varying periodicity. An IC design layout is obtained in step **501**. In step **502** identifying the location of injectors within the design is performed. Step **503** provides the magnitude of current injection for which the system is to be designed to protect against. In step **504** circuit structures are located within the design that are susceptible to latch-up. The location of each latch-up structure may be obtained seriatim, i.e. one-by-one as part of a loop routine configured to operate upon data via a data structure on each iteration, which is suggested by the logic illustrated in the flow diagram.[4]

Evaluation of the distance between each latch-up structure and each injector is accomplished in step **505**. As with step **504**, this determination may be made seriatim, i.e. one-by-one (one latch-up structure, one injector) as part of a loop routine configured to operate upon data via a data structure on each iteration, which is suggested by the logic illustrated in the flow diagram. Step **506** determines the magnitude of current at each latch-up structure. The current at each latch-up structure is, in part, a function of the magnitude of the current provided by the injector, and the distance between the structure and the injector. In step **507**, the resistance of the latch-up structure itself may be employed. Determining the periodicity (L) of contact placement necessary to make a particular structure robust to latch-up is accomplished in step **508**. Given the magnitude of current available at each latch-up structure, as determined in step **506**, and the resistance of the latch-up structure itself, as obtained in step **507**, the quantity of contacts and

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[3] *Id.* at FIG. 6A; paragraph [0058], lines 19-25.
[4] *Id.* at FIG. 5; paragraph [0043], line 1 to paragraph [0046], line 17.

their periodicity of placement is determined for a particular latch-up structure to be latch-up robust.[5]

In addition, steps **507** and **508** may be performed in conjunction with one another to determine both latch-up structure resistance and contact periodicity within the same analytical structure. Step **509** tests for the presence of additional latch-up structures. If there are additional latch-up structures, the process of determining periodicity can be performed for those structures as well. Step **510** tests for the presence of additional injectors. When the contact periodicity (L) necessary to make each latch-up structure robust to latch-up has been determined, an aggregate contact layout will be made for the design **511**. At the conclusion of step **511**, the design of an IC having contacts of varying periodicity is complete.[6]

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. 35 U.S.C. 102(b) rejection of claims 1-10 and 15-31 over US 5,675,170 (Kim et al.)

B. 35 U.S.C. 102(b) rejection of claims 1, 7 and 11-14 over US 4,642,667 (Magee)

VII. ARGUMENT

Legal Principles

The Final Rejection includes rejections based on anticipation. "Anticipation under 35 USC §102(e) requires that 'each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'" *In re Robertson*, 49 USPQ 1949, 1950 (Fed.Cir. 1999).

"All words in the claim must be considered in judging the patentability of the claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970). As set forth in section 2111 of the MPEP, "claims are interpreted in the broadest reasonable

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[5] *Id.* at FIG. 5; paragraph [0047], line 1 to paragraph [0050], line 5.
[6] *Id.* at FIG. 5; paragraph [0051], line 1 to paragraph [0056], line 3.

fashion *consistent with the specification*." (Emphasis added). The Patent and Trademark Office *is required* to take into account whatever enlightenment is afforded by the specification, *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ 2d 1023, 1027-28 (Fed. Cir. 1997). (Emphasis added).

In addition, Applicants note that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[7] *There must be no difference between the claimed invention and reference disclosure* for an anticipation rejection under 35 U.S.C. §102[8] (emphasis added). To properly anticipate a claim, the reference must teach every element of the claim.[9] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[10] "The identical invention must be shown in as complete detail as is contained in the …claim."[11] In determining anticipation, no claim limitation may be ignored.[12]

Applicants respectfully submit the applied art does not meet this threshold burden. In particular, the outstanding Office Action asserts that Kim et al. and Magee discloses all the claimed limitations. Specifically, Applicants respectfully submit that neither Kim et al. nor Magee disclose "an injection site associated with said CMOS semiconductor structure" that is compatible with modern CMOS technologies. Thus, there is a difference between the claimed invention and the reference disclosures of Kim et al. and Magee. Accordingly, this Brief responds to the rejections of the claims on appeal as set forth in the explicit statements of the rejections as noted above. The following paragraphs provide evidence to substantiate these statements.

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[7] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[8] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[9] *See* MPEP § 2131.
[10] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[11] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[12] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

1. The anticipation rejection over Kim et al. is deficient, as the applied art does not disclose all the limitations of claims 1-10 and 15-31.

Kim et al. discloses an apparatus for decreasing latch-up in I/O circuits such as a data output buffer.[13] In particular, Kim et al. discloses an N-well guard ring **4** that is disposed under a data input and output pad **5**.[14] In addition, Kim et al. discloses the N-well guard ring **4** is not only formed on a portion adjacent to the P-well **2** and the N-well **3**, but also *formed on a portion of the P-type substrate under the data output pad* **5**, wherein the N-well guard ring **4** is formed as a single enlarged N-well guard ring (emphasis added).[15]

Further, Kim et al. discloses that the N-well guard ring **4** does not have a separated structure such as the first and the second N-well guard rings **4A** and **4B** in CMOS technologies, but instead has a widely expanded and integrated structure.[16] Moreover, Kim et al. discloses that the minority carriers transmitted from the second N^+ region **23** to the first N^+ pickup region **34** of the PMOS transistor are completely captured by the expanded N-well guard ring **4**, thereby preventing generation of the latch-up in NMOS and PMOS technologies.[17]

However, Kim et al. nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

In addition, claim 22 recites similar language. That is, in contrast to Kim et al., the claimed invention is directed toward a modern CMOS semiconductor structure.

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[13] Kim et al. ABSTRACT.
[14] *Id.* at FIG. 3, FIG. 4, column 2, lines 51-53.
[15] *Id.* at FIG. 3, FIG. 4, column 2, lines 53-56.
[16] *Id.* at FIG. 1, FIG. 2, column 2, lines 58-61.
[17] *Id.* at column 2, lines 61-65.

Further, though Kim et al. discloses an apparatus that decreases latch-up in NMOS and PMOS technologies, it is respectfully submitted that Kim et al. does *not* disclose:

(1) an apparatus with the "CMOS semiconductor structure" of the claimed invention; and

(2) an apparatus that is applicable to modern CMOS technologies.

As discussed above, Kim et al. requires the use of the area under the I/O pad for expanding the N-well guard ring in order to prevent latch-up. In contrast to Kim et al., in the claimed invention and in more modern CMOS technologies *the area under I/O pads is not available because additional circuits are placed under the I/O pads* due to restraints on integrated circuit area and requirements for increased integrated circuit functionality. Due to these restraints and the density requirements of today's integrated circuits, the apparatus for latch-up prevention in Kim et al. is *not* applicable to modern CMOS technologies. Thus, Kim et al. does not disclose the "CMOS semiconductor structure" of the claimed invention and that is required in modern CMOS technologies.

Further, the structure/approach disclosed by Kim et al. of expanding the N-well guard ring to collect injected minority carriers to reduce latch-up is *not applicable* for non-standard latch-up tests "arising from a cable discharge event," as recited in claims 19 and 29. That is, the structure/approach of Kim et al. is not applicable for these latch-up tests because the "injection site associated with said CMOS semiconductor structure" during the recited "cable discharge event" would require an unreasonably large N-Well guard ring in the apparatus of Kim et al. in order to prevent latch-up.

Moreover, the expanded/large N-Well guard rings of Kim et al. would be very difficult to implement in a modern CMOS semiconductor structure because these large/expanded guard rings would increase the size of I/O cells of the integrated circuit and would result in a larger requirement for integrated circuit area for these cells and thus reduce integrated circuit density and functionality.

Therefore, at least for the reasons above, it is respectfully submitted that Kim et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 1 and 22, and claims dependent thereon patentably distinguish thereover.

2. The anticipation rejection over Magee is deficient, as the applied art does not disclose all the limitations of claims 1, 7 and 11-14.

Magee discloses a bipolar lateral transistor that was compatible with "current NMOS or CMOS processing."[18] It should be noted that "current" at the time of the Magee patent disclosure was 1987. In particular, Magee discloses an npn lateral transistor structure that is formed in a very lightly doped p^{--} -type silicon substrate **11**.[19] In addition, Magee discloses a lightly doped n^{-} -type well **12** that is deeply diffused into the substrate **11** and a further lightly doped p^{-} -type well **13** that is diffused into the n^{-} -type well **12**.[20] Further, Magee discloses a p-type region **14** that is diffused to form the intrinsic base, together with a p^{+} -type region to act as a base contact.[21] Furthermore, Magee discloses that N^{+} regions are added for the emitter **16** and collector contact region **17**, during which the emitter is diffused through the same window as the base **14**, to end up with a narrow P region surrounding and self aligned to the emitter. Moreover, Magee discloses the contact region **17** provides a collector for lateral transistor action and a collector contact for vertical transistor action.[22]

However, Magee nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

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[18] Magee at ABSTRACT and column 2, lines 29-35.
[19] Magee at column 1, lines 62-64.
[20] Magee at column 1, lines 64-66.
[21] Magee at column 1, lines 66-68.
[22] Magee at column 2, lines 5-7.

That is, in contrast to the Magee patent issued in 1987, the claimed invention is directed toward modern "CMOS semiconductor structures," as recited in claim 1. As discussed above in regards to Kim et al., it is respectfully submitted that the apparatus and structure of Magee is not applicable to modern CMOS semiconductor structures that have restraints on integrated circuit area and requirements for increased integrated circuit density and functionality.

Further, Magee was directed toward building bipolar transistors in the current CMOS processes of 1987. However, Magee was not directed toward the problem of reducing latch-up in modern CMOS technologies or in the "CMOS semiconductor structure," as recited in claim 1.

Moreover, Magee discloses an arrangement of n+ and p+ taps that is not feasible in a modern "CMOS semiconductor structure" due to space constraints in modern CMOS technologies.[23] Thus, it is respectfully submitted that Magee teaches away from the claimed invention.

Therefore, at least for the reasons above, it is respectfully submitted that Magee does not disclose, anticipate or inherently teach the claimed invention and that claim 1, and claims dependent thereon patentably distinguish thereover.

[23] *Id.* at FIG. 2.

VIII. CLAIMS

A copy of claims 1-31 involved in the present appeal is attached hereto as Appendix A.

In view of the Arguments presented above, reversal of the rejections by the Honorable Board and allowance of pending claims 1-37 is respectfully requested.

Respectfully submitted,

By__/Myron Keith Wyche/__
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Agent for Applicant

APPENDIX A- CLAIMS ON APPEAL

Claims Involved in the Appeal of Application Serial No. 10/605,699

1. A CMOS semiconductor structure comprising:

a substrate;

a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition;

an injection site associated with said CMOS semiconductor structure; and

a plurality of contact regions inter-spaced a varying distance between said circuit structures.

2. The semiconductor structure of claim 1, wherein said distance varies with the proximity of said contact regions to said injection site.

3. The semiconductor structure of claim 1, wherein said distance varies with the susceptibility of said circuit structures to a latch-up condition.

4. The semiconductor structure of claim 1, wherein said plurality of contact regions comprises a first contact region and a second contact region spaced a first distance apart, and said second contact region and a third contact region spaced a second distance apart different from said first distance.

5. The semiconductor structure of claim 4, wherein said first distance is greater than said second distance.

6. The semiconductor structure of claim 4, wherein said first distance is less than said second distance.

7. The semiconductor structure of claim 1, wherein said substrate comprises a well region having formed therein said latch-up susceptible circuit structure.

8. The semiconductor structure of claim 7, wherein said well region is n-type.

9. The semiconductor structure of claim 8, wherein said n-type well region includes at least one contact comprising an n+ region.

10. The semiconductor structure of claim 9, wherein said at least one contact is coupled to Vdd.

11. The semiconductor structure of claim 7, wherein said well region is p-type.

12. The semiconductor structure of claim 11, wherein said p-type well region includes at least one contact comprising a p+ region.

13. The semiconductor structure of claim 12, wherein said at least one contact is coupled to ground.

14. The semiconductor structure of claim 12, wherein said at least one contact is coupled to Vss.

15. The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged vertically relative to said axis.

16. The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged horizontally relative to said axis.

17. The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged concentrically relative to said axis.

18. The semiconductor structure of claim 1, wherein said distance is determined such that said latch-up susceptible circuit structure is prevented from latching-up when carriers are injected into the substrate from an external current injector.

19. The semiconductor structure of claim 18, wherein said external current injector is a cable discharge arising from a cable discharge event.

20. The semiconductor structure of claim 1, wherein said distance increases as the distance of said plurality of contact regions from said injection site increases.

21. The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from said injection site increases.

22. A method of forming a CMOS semiconductor structure having improved latch-up robustness, the method comprising the steps of:

providing a substrate including an injection site associated with said CMOS semiconductor structure and a plurality of circuit structures, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; and

forming a plurality of contact regions inter-spaced a varying distance between said circuit structures.

23. The method of claim 22, wherein said distance varies with the proximity of said plurality of contact regions to said injection site.

24. The method of claim 22, wherein said distance varies with the susceptibility of said circuit structures to a latch-up condition.

25. The method of claim 22, wherein said step of forming comprises forming a first contact region and a second contact region spaced a first distance apart, and said second contact region and a third contact region spaced a second distance apart different from said first distance.

26. The method of claim 25, wherein said first distance is greater than said second distance.

27. The method of claim 25, wherein said first distance is less than said second distance.

28. The method of claim 22, wherein said distance is determined such that said latch-up susceptible circuit structure is prevented from latching-up when carriers are injected into the substrate from an external current injector.

29. The method of claim 28, wherein said external current injector is a cable discharge arising from a cable discharge event.

30. The method of claim 22, wherein said distance increases as the distance of said plurality of contact regions from said injection site increases.

31. The method of claim 22, wherein said plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from said injection site increases.

APPENDIX B – EVIDENCE

NONE

APPENDIX C - RELATED PROCEEDINGS

NONE